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AD6311

1/8- to 1/16 Duty VFD Controller/Driver

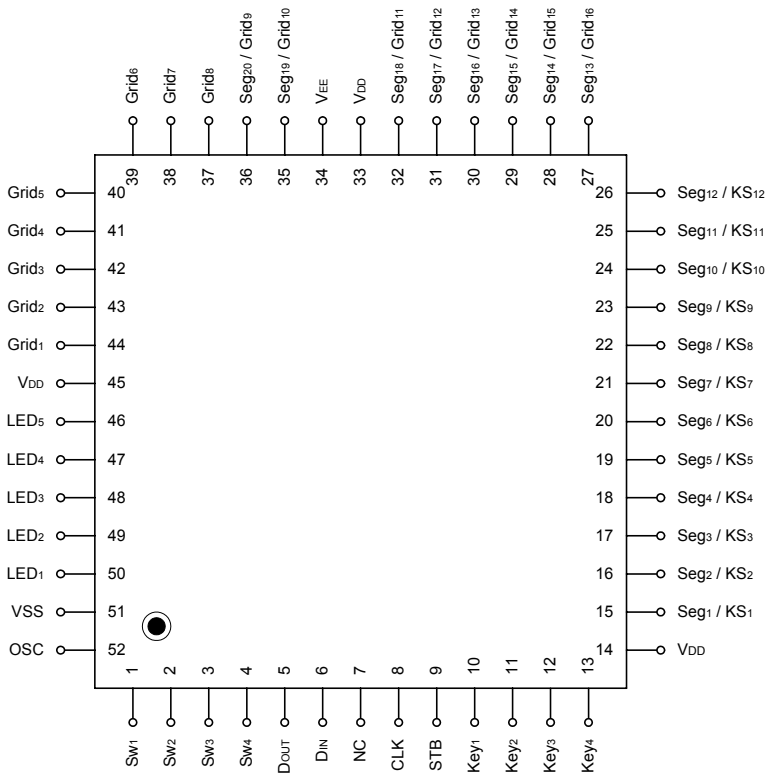
■ Features

- 4-pin serial interface
- Key scanning (12x4 matrices)
- Programming display modes (16-digit & 12-segment to 8-digit & 20-segment)
- Programming dimming step
- High-voltage output (V_{DD}-35V max)
- 5 channels LED ports
- 4-pin general-purpose input port
- Built-in oscillator
- No external resistor necessary for driver outputs

■ General Description

The AD6311 is a VFD (Vacuum Fluorescent Display) controller/driver that is driven on a 1/8- to 1/16 duty factor (include key scan). It consists of 12 segment/key scan output lines, 8 grid output lines, 8 segment/grid output drive lines, a display memory, a control circuit, and a key scan circuit. Serial data is input to the AD6311 through a four-line serial interface.

■ Pin Assignments



Use all the power pins.

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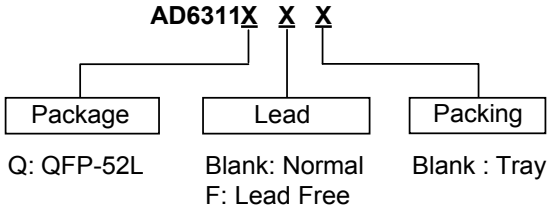
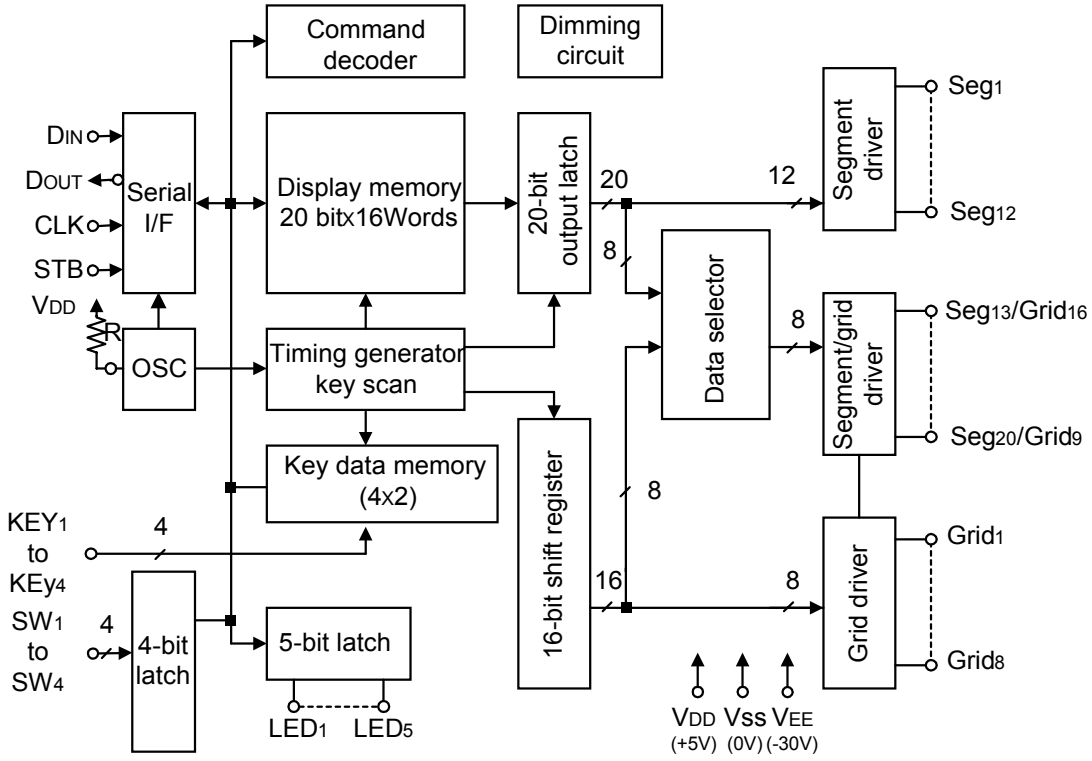
■ Pin Descriptions

Symbol	Name	No.	Description
D_{IN}	Data input	6	Input serial data at rising edge of shift clock, starting from the low order bit.
D_{OUT}	Data output	5	Output serial data at the falling edge of the shift clock, starting from low order bit. This is N-ch open-drain output pin.
STB	Strobe	9	Initializes serial interface at the rising or falling edge of the AD6311. It then waits for reception of a command. Data input after STB falling is processed as a command. While command data is processed, current processing is stopped, and the serial interface is initialized. While STB is high, CLK is ignored.
CLK	Clock input	8	Reads serial data at the rising edge, and outputs data at the falling edge.
OSC	Oscillator pin	52	Connect resistor in between this pin and Vdd to set up the oscillation frequency.
Seg_1/KS_1 to Seg_{12}/KS_{12}	High-voltage output	15 to 26	Multi-function pins, Segment output pins (Dual function as key scan source)
$Grid_1$ to $Grid_8$	High-voltage output (Grid)	37 to 44	Grid output pins
$Seg_{13}/Grid_{16}$ to $Seg_{20}/Grid_9$	High-voltage output (Segment/grid)	27 to 32 35, 36	These pins are selectable for segment or grid driving.
LED_1 to LED_5	LED output	46 to 50	CMOS output
KEY_1 to KEY_4	Key data input	10 to 13	Data input to these pins is latched at the end of the display cycle.
V_{DD}	Logic power	14, 33, 45	Logic power supply
V_{SS}	Logic ground	51	Connect this pin to system GND.
V_{EE}	Pull-down level	34	Driver power supply
SW_1 to SW_4	Switch input	1 to 4	These pins constitute a 4-bit general-purpose input port.
NC	NC	7	No connection

■ Ordering Information



■ Block Diagram



■ Absolute Maximum Ratings (T_A=25℃,V_{SS}=0V)

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{DD}	-0.5 to +7.0	V
Driver supply voltage	V_{EE}	V_{DD} +0.5 to V_{DD} -40	V
Logic input voltage	V_{I1}	-0.5 to V_{DD} +0.5	V
VFD driver output voltage	V_{O2}	V_{EE}-0.5 to V_{DD} +0.5	V
LED driver output current	I_{O1}	+15	mA
VFD driver output current	I_{O2}	-40(grid) –15 (segment)	mA
Operating ambient temperature	T_{OPT}	-25 to +85	℃
Storage temperature	T_{STG}	-50 to +125	℃

■ Operating Conditions (T_A=0 to +70℃,V_{SS}=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logic supply voltage	V_{DD}		4.5	5	5.5	V
High-level input voltage	V_{IH}		0.7·V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL}		0		0.3xV_{DD}	V
Driver supply voltage	V_{EE}		0		V_{DD}-35	V

■ DC Characteristics (T_a=0 to 70℃, V_{DD}=4.5 to 5.5V, V_{SS}=0V, V_{EE}=V_{DD}-35V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level output voltage	V_{OH1}	LED_1-LED_5,I_{OH1}=-1mA	0.9V_{DD}			V
Low-level output voltage	V_{OL1}	LED_1-LED_5,I_{OL1}=12mA			1	V
Low-level output voltage	V_{OL2}	D_{OUT},I_{OL2}=2mA			0.4	V
High-level output current	I_{OH21}	V_O=V_{DD}-2V,Seg_1 to Seg_{12}	-3			mA
High-level output current	I_{OH22}	V_O=V_{DD}-2V,$Grid_1$ to $Grid_8$, Seg_{13}/$Grid_{16}$ to Seg_{20}/$Grid_9$	-15			mA
Driver leakage current	I_{OLEAK}	V_O=V_{DD}-35V, driver off			-10	μA
Output pull-down resistor	R_L	Driver output	50	100	150	kΩ
High-level input voltage	V_{IH}		0.7V_{DD}			V
Low-level input voltage	V_{IL}				0.3V_{DD}	V

■ AC Characteristics (T_a=0 to +70℃,V_{DD}=4.5 to 5.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC}	R=51 kΩ	350	500	650	KH_Z
Maximum clock frequency	$f_{max.}$	Duty=50%			1	MH_Z
Clock pulse width	PW_{CLK}		500			ns
Strobe pulse width	PW_{STB}		1			μs
Data setup time	t_{SETUP}		100			ns
Data hold time	t_{HOLD}		100			ns
Clock-strobe time	$t_{CLK-STB}$	CLK ↑ →STB ↑	1			μs
Wait time	t_{WAIT}	CLK ↑ →CLk ↓ (Note)	1			μs

Note: Refer to page 8.

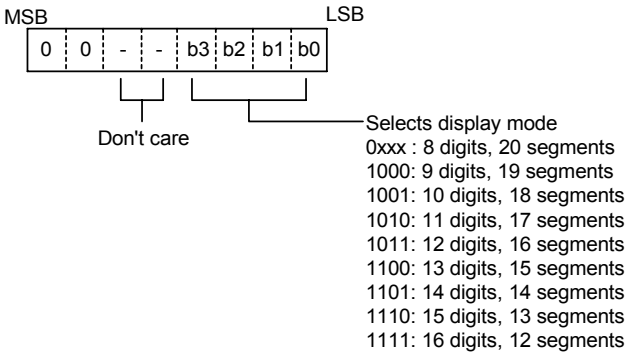
■ Function Description

1.0 Command

A command sets the display mode and status of the VFD driver. The first 1 byte input to the AD6311 through the Din pin after the STB pin has fallen is regarded as a command. If STB is made high while a command/data is transmitted, serial communication is initialized, and the command/data being transmitted is invalid (however, the command/data already transmitted remains valid).

1.1 Display mode setting command

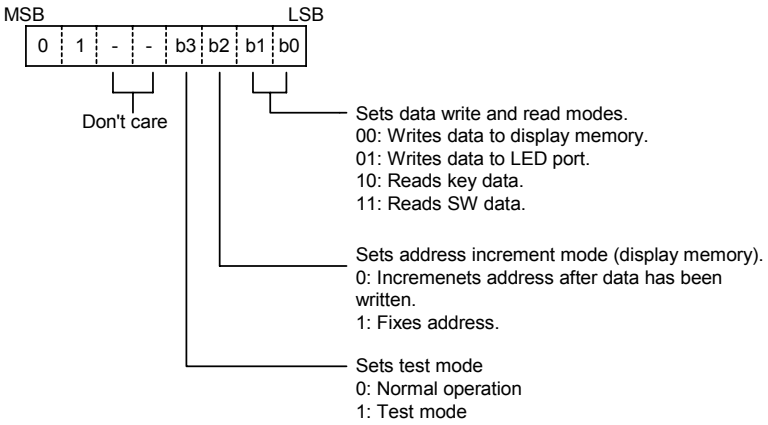
This command initializes the AD6311 and selects the number of segments and number of grids (8 grid & 20 segments to 16 grid & 12 segments). When this command is executed, display is forcibly turned off, and key scanning is also stopped. To resume display, a display ON command must be executed. If the same mode is selected, however, nothing is performed.


MSB
LSB
0 0 - - b3 b2 b1 b0
Don't care
Selects display mode
0xxx : 8 digits, 20 segments
1000: 9 digits, 19 segments
1001: 10 digits, 18 segments
1010: 11 digits, 17 segments
1011: 12 digits, 16 segments
1100: 13 digits, 15 segments
1101: 14 digits, 14 segments
1110: 15 digits, 13 segments
1111: 16 digits, 12 segments

On power application, the 16-digit, 12-segment mode is selected.

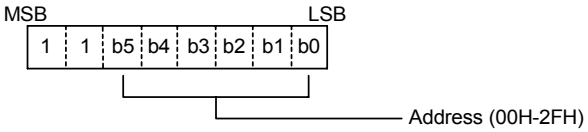
1.2 Data setting command

This command sets data write and data read modes. On power application, the normal operation mode and address increment mode are set.

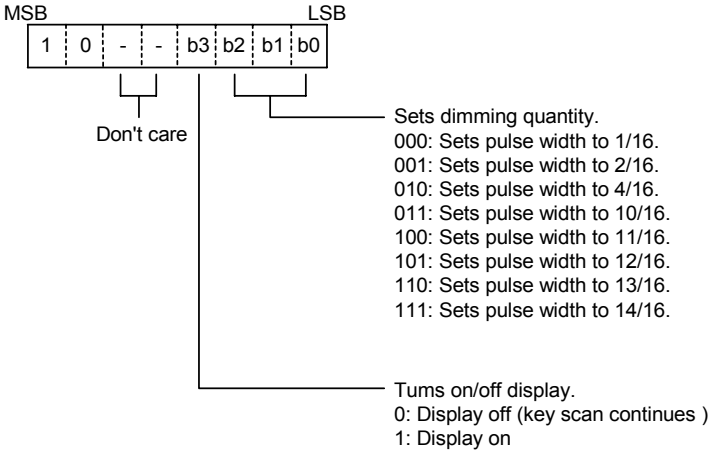

MSB
LSB
0 1 - - b3 b2 b1 b0
Don't care
Sets data write and read modes.
00: Writes data to display memory.
01: Writes data to LED port.
10: Reads key data.
11: Reads SW data.
Sets address increment mode (display memory).
0: Incremenets address after data has been written.
1: Fixes address.
Sets test mode
0: Normal operation
1: Test mode

1.3 Address setting command

This command sets an address of the display memory. If address 30H or higher is set, the data is ignored, until a correct address is set. On power application, the address is set to 00H.



1.4 Display control command



On power application, the 1/16-pulse width is set, the display is turned off and key scanning is stopped.

2.0 Display RAM Address and Display Mode

The display RAM stores the data transmitted from an external device to the AD6311 through the serial interface, and is assigned addresses as follows, in units of 8 bits:

Seg_1	Seg_4	Seg_8	Seg_{12}	Seg_{16}	Seg_{20}	
00 H_L	00 H_U	01 H_L	01 H_U	02 H_L		$GRID_1$
03 H_L	03 H_U	04 H_L	04 H_U	05 H_L		$GRID_2$
06 H_L	06 H_U	07 H_L	07 H_U	08 H_L		$GRID_3$
09 H_L	09 H_U	0 AH_L	0 AH_U	0 BH_L		$GRID_4$
0 CH_L	0 CH_U	0 DH_L	0 DH_U	0 EH_L		$GRID_5$
0 FH_L	0 FH_U	10 H_L	10 H_U	11 H_L		$GRID_6$
12 H_L	12 H_U	13 H_L	13 H_U	14 H_L		$GRID_7$
15 H_L	15 H_U	16 H_L	16 H_U	17 H_L		$GRID_8$
18 H_L	18 H_U	19 H_L	19 H_U	1 AH_L		$GRID_9$
1 BH_L	1 BH_U	1 CH_L	1 CH_U	1 DH_L		$GRID_{10}$
1 EH_L	1 EH_U	1 FH_L	1 FH_U	20 H_L		$GRID_{11}$
21 H_L	21 H_U	22 H_L	22 H_U	23 H_L		$GRID_{12}$
24 H_L	24 H_U	25 H_L	25 H_U	26 H_L		$GRID_{13}$
27 H_L	27 H_U	28 H_L	28 H_U	29 H_L		$GRID_{14}$
2 AH_L	2 AH_U	2 BH_L	2 BH_U	2 CH_L		$GRID_{15}$
2 DH_L	2 DH_U	2 EH_L	2 EH_U	2 FH_L		$GRID_{16}$

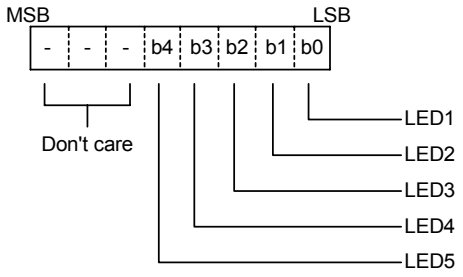
b0	b3 b4	b7
XX H_L	XXH_U	

Lower 4 bits Higher 4 bits

Only the lower 4 bits of the addresses assigned to Seg_{17} through Seg_{20} are valid, and the higher 4 bits are ignored.

3.0 LED Port

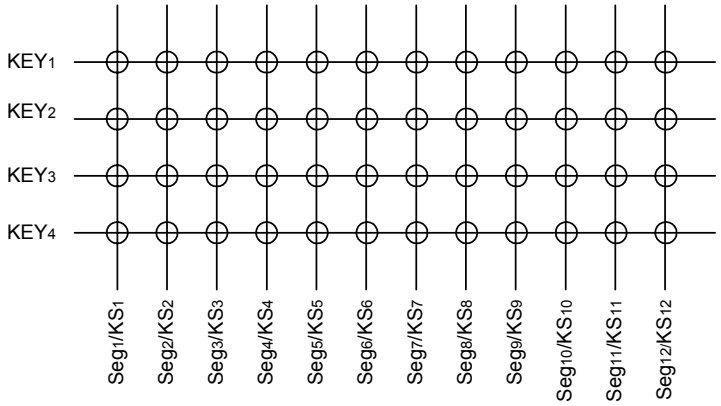
Data is written to the LED port by a write command, starting from the least significant bit of the port. When a bit of this port is 0, the corresponding LED lights; when the bit is 1, the LED goes off . The data of bits 6 through 8 is ignored.



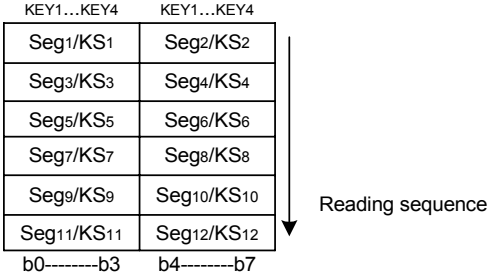
On power application, all the LEDs remain dark.

4.0 Key Matrix and Key-Input data Storage RAM

The key matrix is of 12x4 configuration, as shown below.

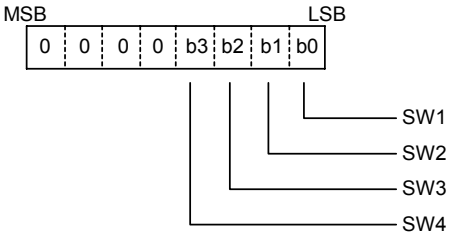


The data of each key is stored as illustrated below, and is read by a read command, starting from the least significant bit. When the most significant bit of data (Seg_{12} b_7) has been read, the least significant bit of the next data (Seg_1 b_0) is read.



5.0 SW Data

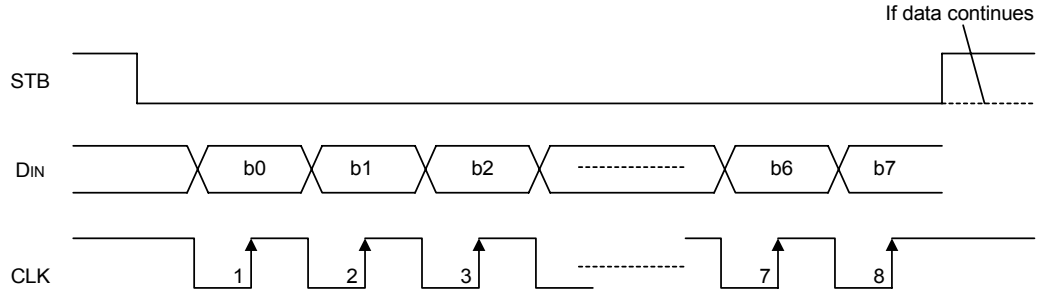
The SW data is read by a read command, starting from the least significant bit. Bits 5 through 8 of the SW data are 0.



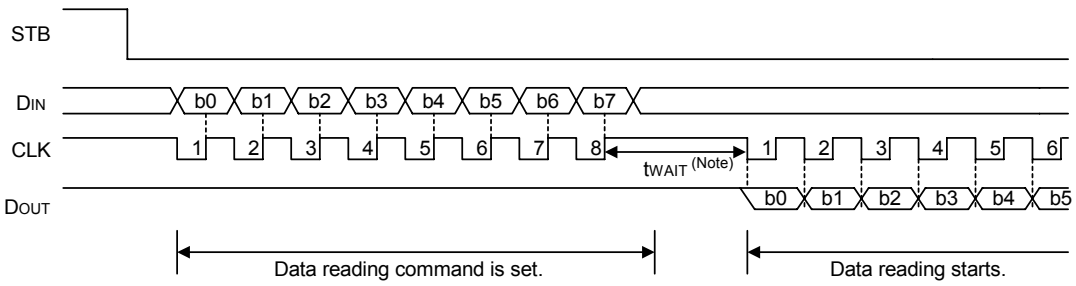
■ Timing Diagram

(1) Serial Communication Format

Reception (command/write data)



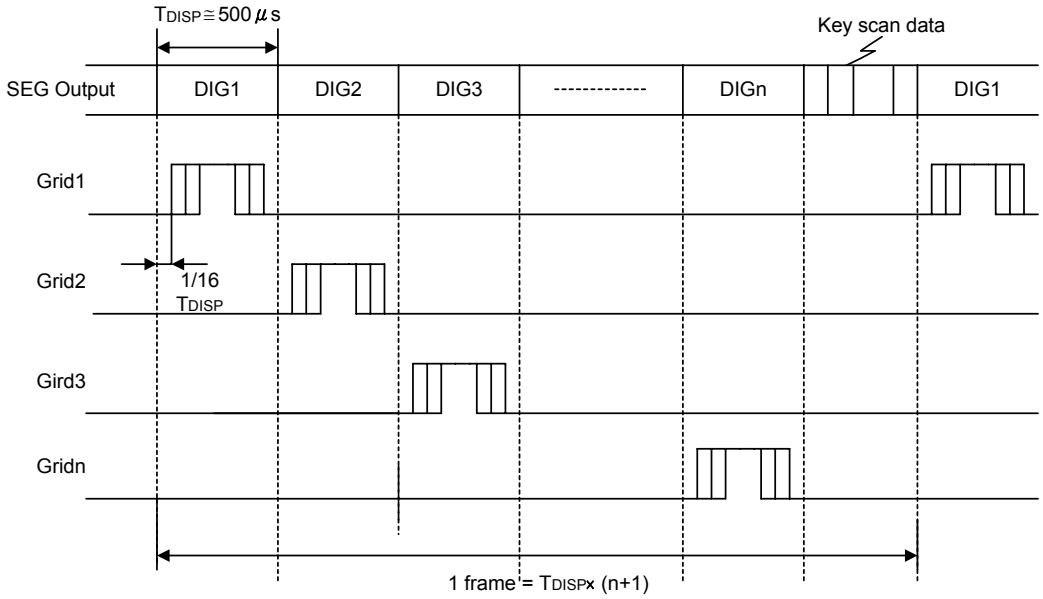
Transmission (read data)



Because the D_{OUT} pin is an N-ch, open-drain output pin, be sure to connect an external pull-up resistor to this pin (1kΩ to 10 kΩ).

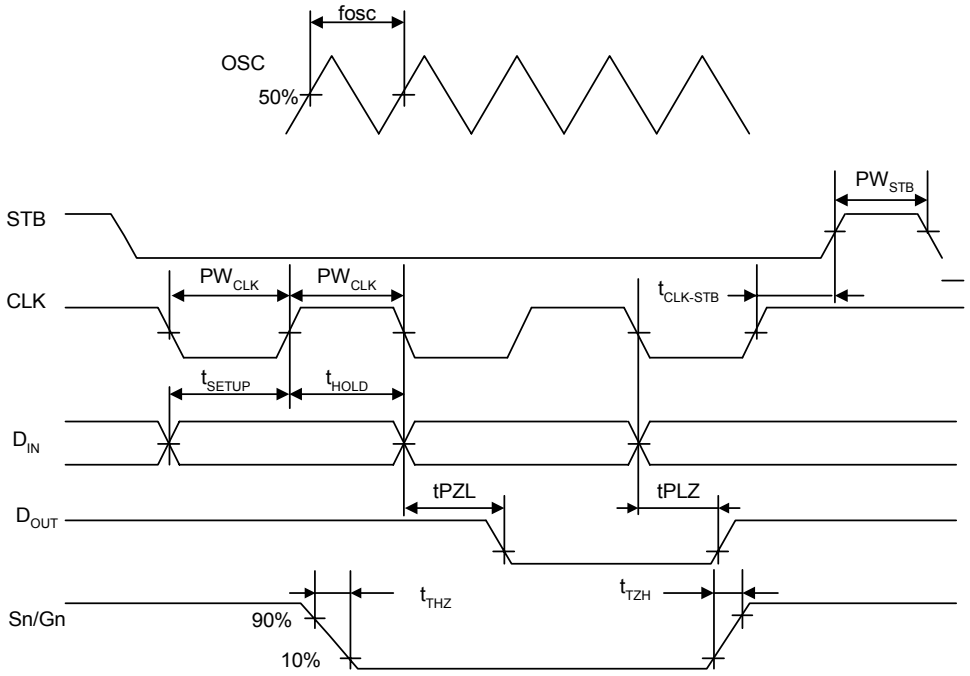
Note : When data is read, a wait time t_{WAIT} of 1 μs is necessary since the rising of the eighth clock that has set the command, until the falling of the first clock that has read the data.

(2) Key Scanning and Display Timing



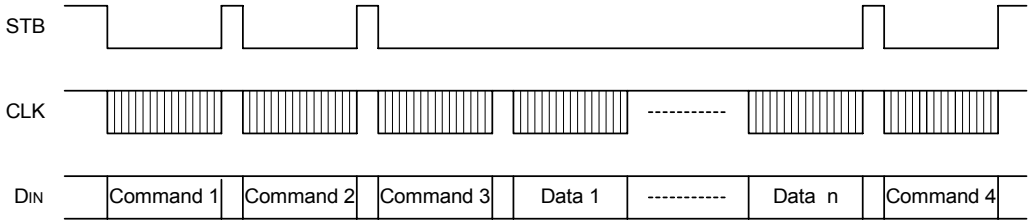
One cycle of key scanning consists of two frames, and data of 12× 4 matrices is stored in RAM.

AC characteristic waveform



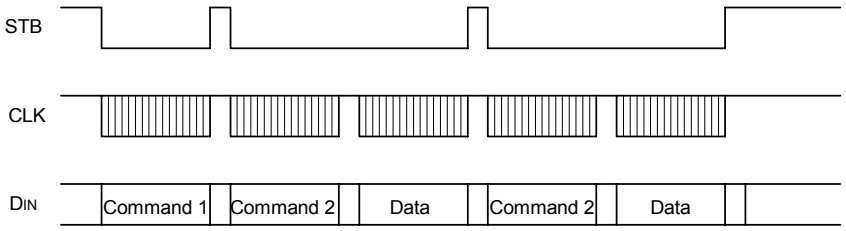
Applications

Updating display memory by incrementing address



Command 1: sets display mode
Command 2: sets data(write data to display memory)
Command 3: sets address
Data 1 to n: transfers display data (48 bytes max.)
Command 4: controls display

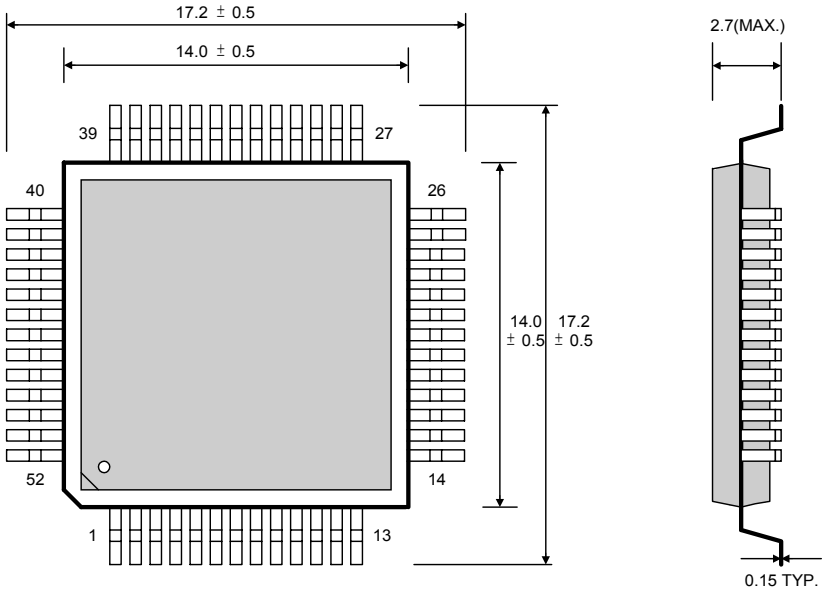
Updating specific display memory

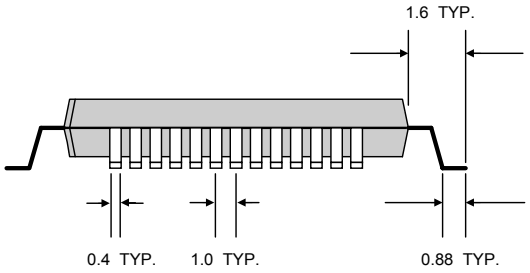


Command 1: sets data
Command 2: sets address
Data: display data

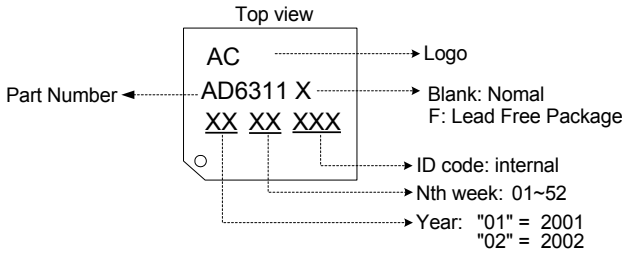
■ Package Information

52 pins QFP dimension Unit: mm





■ Marking Information



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